Exhibit 17

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Minutes of Meeting No. 163
JC-40 Digital Logic Committee

September 16, 2010 **Denver, Colorado**

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1.0 JC-40 Digital Logic Plenary

The JC-40 Plenary meeting opened at 8:18 AM on September 16, 2010. Mr. Smolka led the discussions of this group.

Self-introductions were completed by the attendees.

1.1.0 Patent Policy

The patent policy was reviewed.

1.2.0 Minutes

Mr. Kellogg identified two corrections to the June 2010 JC-40 meeting minutes:
- In section 3.2.1.0, the name associated with ballot #JC-40.3-10-97 should be "DDR3U Register" instead of "DDR3 Register".

- The date for legal approval of the minutes is listed as "June 16, 2006", and should be "June 16, 2010".

The minutes of the June 2010 meeting were reviewed and approved with the proposed modifications from the meeting secretary, Mr. Kellogg, with a motion by Montage and seconded by IBM.
The motion passed by acclamation.

1.3.0 Agenda

The agenda was reviewed.

1.4.0 BoD Ballot Review

Mr. Smolka reviewed BoD ballot #JCB-10-38 BoD (Committee item #150.01, JC-40 Policies – Meeting Start Time). A question was asked

during the BoD balloting in regard to the resolution of the Silego and TI comments.

- Mr. Smolka asked Silego if their comment to the committee ballot was addressed: Response: Yes.
- Mr. Smolka asked TI if their comment to the committee ballot was addressed: Response: Yes.

2.0 JC-40.1 CMOS/BiCMOS Digital Logic

The JC-40.1 meeting opened at 8:26 AM on September 16, 2010. Mr. Williams led the discussion of this group.

2.1.0 Agenda

The agenda was reviewed. There were no ballots or member showings.

2.2.0 Task Group Update

2.2.1.0 #121.00 TG JEDEC Instrumentation Chip TG Status

The instrumentation chip specification was found to require several modifications which were reviewed in the March '10 meeting. A ballot was authorized at that time, but not issued.

The proposed changes were presented to the committee at this time. The specification included several proposed modifications in red text – most of which resulting when the original source file was converted to Framemaker for publication.

Discussion:
- Change "K" to lower case in "kHz". Response: Accepted.

Mr. Williams agreed to provide the updated file to the JEDEC office.

Motion by Montage and seconded by HP to accept the proposed specification modifications as being editorial.
The motion passed by acclamation.

Motion by Oracle and seconded by Silego to close TG.
The motion passed by acclamation.

The TG was closed.

3.0 JC-40.3 RDIMM Support Devices

The JC-40.3 meeting opened at 8:34 AM on September 16, 2010. Mr. Ammar led the discussions of this group.

3.1.0 Agenda

The agenda was reviewed and updated. There were no ballots or second presentations.

3.2.0 First Presentations

3.2.1.0 #FYI TI DRAM Input Inversion for DDR4

TI indicated that the material was shown as item #1716.80 in JC-42.3 and is being shown in this committee as an informational showing.

TI is requesting DDR4 DRAMs to include the capability to allow inversion of all register "B" outputs (address, control and command inputs to DRAMs) upon initial power-up.

Higher DDR4 speeds mandate signaling improvements over DDR3 – the main detractors were summarized, including SSO and cross-talk. The source of the register SSO effects were listed, followed by a register device diagram identifying the SSO contributors.

Shortcomings of DDR3 output inversion were listed – including the small number of inputs allowing inversion (14 of 28), the distance between the signals, neighbor trace coupling, etc.

The design of a register package with much lower power inductance or the adoption of a different signaling scheme (e.g. differential) would be another means of improving signaling.

A permanent inversion solution for DDR4 memory devices was identified as the optimal solution to enable maximum performance for applications requiring register devices. Other possible benefits were listed for

consideration.

Discussion:
- Register timings will be a critical aspect for DDR4 – some solution is required at the DRAM level to enable the register to meet the required performance.
- The DDR4 register may need to change if the DRAM changes. JC-40 member participation was requested in the DDR4 Signaling TG.

3.2.2.0 #FYI TI Request for DDR4 DRAM to Ignore MR7 Bits

TI indicated that the material was shown as item #1716.81 in JC-42.3 and is being shown in this committee as an informational showing.

TI summarized the controller and registers need to include additional complexity to allow for register control word access. The current implementation also adds latency to the register.

An alternate solution was proposed in which the register would simply monitor information passing across the bus to the register, and use the bus information to program the register upon detection of a MR7 command to the DRAM. The DRAM would ignore MR7 commands – which would be reserved for use by the register.

Upon consideration of the proposal, JC-42.3 recommended that the register use MR15 commands instead of MR7. Although MR15 is not operational on x16 DRAMs, x16 DRAMs are not used on existing registered DIMMs anyway.

Discussion:
- A member suggested that x16 devices may be used on DDR4 registered small outline DIMMs – since small outline RDIMMs using x16 DDR3 DRAMs exist currently.
- The DDR4 functions and features TG will need to decide which MR might be shared with the register.

3.2.3.0 #31.07 Silego tDYNOFF and tSTAOFF Definition in JESD65

The proposed modifications to JESD65 were shown, to add tDYNOFF and tSTAOFF. The information was extracted from the SSTE32882 specification.

Motion by Silego and seconded by (no second) to elevate the material to be considered as a second showing.
There was at least one member objection, so the material was not elevated.

3.2.4.0 #157.00 AMD DDR3 3DS Stack Register

The DDR3 3DS SDRAM addressing was covered in JC-42.3. The register operation, including rank multiplication modes, was reviewed. AMD requested consideration of these modes in a DDR3 3DS register.

Discussion:
- Other features will be requested in the register to operate the 3DS stacked package.
- Electrical characteristics will also be affected on the register.
- The register control words will be affected.
- Rather than modify the SSTE32882 specification, it may make more sense to base the implementation on the memory buffer specification.
- The memory buffer (tPDM) specification needs to be improved if the memory buffer specification is used as a base.
- 3DS must operate at 3 DIMMs/channel on same channel with RDIMMs and must have power envelope of a register – not of a memory buffer. It isn't important where the work is done within JC-40.

The chairman indicated that the 3DS work will be done in the Register and PLL TG for now.

3.3.0 Task Group Update

3.3.1.0 #122.00 TG DDR3 Register and PLL TG

The TG logistics were shown, including the website information and conference call information. Recent activities were reviewed, including recent ballots, showings made today, DDR4 register fundamentals, DDR3 tPDM, etc.

The recent committee and BoD ballot results were shown. Future discussion topics were summarized, including DDR4 specifications and DDR3-2133 specification definition.

4.0 JC-40.4 FBDIMM Support Devices

The JC-40.4 meeting opened at 9:19 AM on September 16, 2010. Mr.

Chung led the discussion of this group.

4.1.0 Agenda

The agenda was reviewed and updated.

The agenda included a list of the pass/hold ballots for the DDR3 memory buffer – Mr. Tsang agreed to review the table for completeness.

4.2.0 Ballot Review

4.2.1.0 #142.55A JC-40.4-10-121A LRDIMM DDR3 Memory Buffer Specification Electrical Chapter

The vote count was 15 yes, 0 no and 9 abstentions.

Yes comments:
- AMD: TG needs to continue to work on items in background section – will want to have a motion to this effect.
AMD agreed that their comment was addressed.

- FormFactor: On page 10 note “a”, change from “cap” to “capacitance”.
The committee agreed by acclamation that the comment was addressed.

- Intel: Error in table 5 (not part of ballot material) – “ua” became “ma” when ballot prepared.
Intel agreed that their comment was addressed.

- Micron: Several clarification questions were identified:
1) “tSTAOFF” is shown as an average, but then defines min/max timing.
Response: Need to remove “average” from the parameter definition.
2) Clarify “tPDM range” (Figure 12, footnote b) is this valid for a single register or does it for cover the full possible range? Response: The table includes process, temperature and voltage variation, whereas the identified footnote only applies to one single die - including the voltage and temperature variation. This needs to be clarified in the footnote.
Micron agreed that their comment was addressed.

Patent disclosure:
- Netlist: Netlist disclosed that they may have IP related to this ballot material. Mr. Martinez agreed to provide a letter consistent with the JEDEC policy prior to the December meeting.

Secr. note: Mr. Martinez provided patent and patent application numbers later in the meeting – the numbers are listed in section 4.4.2.0.

Motion by Montage and seconded by *(no second)* to return the material to the TG and to authorize the TG to re-ballot the material to address the comments identified in the ballot voting results.

The motion was withdrawn.

Motion by Montage and seconded by Intel to place the ballot material on pass/hold as-is and to authorize the TG to issue one or more ballots to address the comments identified in the ballot voting results – including the AMD comments related to topics in the background of the ballot material.
The motion passed by acclamation.

4.2.2.0 #142.43 JC-40.4-10-190 DDR3 LRDIMM Memory Buffer Specification MemBIST Chapter

The vote count was 14 yes, 0 no and 9 abstentions.

Yes comments:
- IDT: No registers for MEMBIST failure rank logging, failure address logging concern (also MEMBIST). Ambiguity in section 1.47 vs. other descriptions in specification.
Response: The rationale for the MEMBIST failure logging operation was described – if changes are requested, they will need to be discussed. Also open to discussions regarding the 3rd comment.
IDT agreed that their comment was addressed.

Patent disclosure:
- Netlist: Same disclosure and action as ballot #10-121A.

The ballot material was left on pass/hold as-is.

Motion by Montage and seconded by IDT to authorize the TG to issue one or more ballots specifically to address the items identified in the IDT ballot comments.
The motion passed by acclamation.

4.2.3.0 #142.50A JC-40.4-10-26A DDR3 LRDIMM Memory Buffer Specification Reset Chapter

The vote count was 16 yes, 0 no and 9 abstentions.

Yes comments:
- Texas Instruments: Request a table defining which outputs and settings are affected by the different reset types. Response: A table can be added – Inphi offered to do this.
TI agreed that their comment was addressed.

Abstain comment:
- Viking: No strikethroughs in ballot material: Response: They are there, just hard to see. Response: Resolved.

Motion by Intel and seconded by Montage to place the material on pass/hold as-is and to authorize the TG to issue one or more ballots on the material to address the TI comment.
The motion passed by acclamation.

4.3.0 Second Presentations

4.3.1.0 #156.00 Silego JC-40.4 Guidelines – File Naming

Mr. Chung showed the file naming and item number families that he would like used within the sub-committee. He further identified several numbers to be closed.
- Item #151.01 was reassigned to a new item number family and given item #311.02, and would continue to be considered as a 2nd showing.
- Item #151.02 was reassigned to a new item number family and given item #311.03, and would continue to be considered as a 2nd showing.

4.3.2.0 #142.62 Intel DDR3 LRDIMM Memory Buffer (MB) Specification

The proposed specification was identified as revision 0.9, including all pass/hold ballots as well as all approved editorial changes. The specification includes bookmarks, contents, table and figure listings, and was structured after the AMB specification.

The de-rating table entries previously requested by Elpida were shown, including the "TBD" entries for slew rates slower than 1 V/ns.

Motion by Intel and seconded by Montage to authorize the TG to make editorial changes to the material, include other MB ballot material being issued during the voting period, and issue a ballot for counting in December.

Discussion:
- Is there more material to be added to the specification, other than the 3 ballots previously discussed? Response: No.
- If the committee intends to send the ballot to the BoD in February, should a justification ballot be issued at this time? Response: Yes.

The motion passed by acclamation

Motion by Intel and seconded by Oracle to issue a justification ballot to be counted in December on the full DDR3 MB specification.
The motion passed by acclamation.

The MB IP tracking list was shown.

4.4.0 First Presentations

4.4.1.0 #142.61 Intel Next Generation MB+ for >128MB 3DS modules

In order to support 8-high device configurations, the memory buffer will need to be modified. A list of "3D Stacked DIMM Types and Capacities" was shown identifying some of the areas of concern. The presentation also included structures (in dark green) which need to be addressed by a new register. Both needs could likely be met by a single device if activity is done jointly within JC-40.3 and JC-40.4.

Mr. Smolka agreed that the two affected TGs would discuss the topic.

Discussion:
- Lower density configurations might also be supported by the proposed device. Response: This is not the intent of the device.

Netlist: May have IP that addresses the extensions to the MB to meet the objectives defined in the presentation. Mr. Martinez agreed to provide a letter consistent with the JEDEC policy prior to the December meeting.

Secr. note: Mr. Martinez provided patent and patent application numbers later in the meeting – the numbers are listed in section 4.4.2.0.

Motion by HP and seconded by IBM to elevate the material to be considered as a second showing.
The motion failed as at least one company was opposed.

4.4.2.0 #FYI Google Update to IP Disclosures

Google indicated that the material shown includes both earlier and new IP disclosures – with corrections to prior disclosures. Google also found some new IP that may read on the LRDIMM MB – which is included in this matrix.

Mr. Chung agreed to update the IP Tracking List to reflect the updates.

Discussion:
- Mr. Martinez provided the following patent and patent application numbers relating to the Netlist disclosures made earlier in this meeting: 7,619,912, 7,636,274, 61/186,799, 12/761,179, 12/577,682, and 12/629,827.

4.5.0 Task Group Update

4.5.1.0 #142.10/151.00 TG DDR3/DDR4 MB TG Report

The DDR3/DDR4 MB TG structure and meeting times were shown (an error was identified in the meeting times, which the TG chairman agreed to correct). The current quarter committee ballots were summarized, followed by the TG consensus items and the IP tracking list.

5.0 JC-40.5 Logic Verification and Validation

The JC-40.5 meeting opened at 10:35 AM on September 16, 2010. Mr. Chung led the discussion of this group (Mr. Keller was not present).

5.1.0 Agenda

The agenda was reviewed and updated.

5.2.0 Ballot Review

5.2.1.0 #133.07 JC40.5-10-267 tPDM Measurement Procedure

The vote count was 10 yes, 0 no and 7 abstentions.

Yes comments:
- TI: Technically, the procedure is OK, however the parameter is redundant since it is covered by tSTAOFF and tQsk1. Would like to remove the parameter from the specification to reduce test and validation time.
TI indicated that their comment was addressed.

Motion by Silego and seconded by IDT to submit the tPDM measurement procedure to the BoD.

Discussion:
- A concern was raised by Mr. Smolka that the ballot did not follow the committee policy regarding the ballot closure date. He recommended that no action be taken on the ballot until the December meeting – so that no concerns arise during BoD voting in relation to the committee ballot period.

The motion was withdrawn.

The ballot was left on pass/hold.

5.3.0 Second Presentations

5.3.1.0 #133.08 Agilent tSU/tH Measurement Procedure

The TG discussions have covered measurement procedures and errors in the measurement procedures using different setups. Skew compensation, Rj removal, skew and other sources of errors were summarized – potentially adding well over 10 ps in measurement error.

Motion by Agilent and seconded by Silego to authorize the TG to issue one or more ballots on the material.
The motion passed by acclamation.

5.3.2.0 First Presentations

There were no first presentations in this sub-committee.

5.4.0 Task Group Update

5.4.1.0 #133.00 TG DDR3 Register/PLL Validation TG Report

The TG logistics were shown, with weekly meetings being held. The tPDM ballot was issued, and the tSU/tH procedure ballot will be issued for counting in December.

The TG needs to determine if additional parameters need to be evaluated.

5.4.2.0 #149.04 TG MB Validation TG

The TG logistics were shown – meetings are held weekly, with attendance of 4-8 members on each call. The consensus list items were shown, with no recent updates.

Current TG activity was summarized, with planned TG work to include development of functional and parametric requirements for platforms, consideration of a new method for Cin measurement, review of existing DDR3 DRAM/module validation test, etc.

5.5.0 Other Sub-Committee Discussions

A concern was raised regarding an apparent unavailability of the DDR3 MB Test Card (item #149.06) – which was to be provided to CST for possible production subsequent to the March, 2010 committee meeting. The commitment to provide the information to CST was again recorded in the June, 2010 meeting (as confirmed by Mr. Kellogg).

Discussion:
- Inphi indicated that they had previously informed the committee that the required material would be provided to CST for production – however, straw polls of members at prior meetings did not indicate interest in the procurement of the completed boards from CST – so no action was taken to-date. Inphi indicated that the material would be provided to CST, independent of the identified committee interest level.

Mr. Chung requested a show of hands from members interested in at least one DDR3 MB test board.
- 5 companies indicated interest.

6.0 JC-40 Committee Wrap-Up Mr. Smolka

Mr. Smolka reviewed the remaining agenda material, including the next meeting location (San Francisco), the New Members' Lunch, etc.

6.1.0 JC-40 TG Structure and Chairmanships

Mr. Kellogg reviewed the JC-40 TG structure and chairmanship roles, as updated during the committee meeting.

7.0 Adjournment

Motion by Montage and seconded by Silego to adjourn the meeting. The motion passed by acclamation.

The meeting adjourned at 11:12 AM on September 16, 2010

THIS MEETING WAS CONDUCTED IN ACCORDANCE WITH JEDEC LEGAL GUIDES, JM5, AND THE JEDEC MANUAL OF ORGANIZATION AND PROCEDURE, JM21-P.

REVIEWED/CORRECTED AND AUTHORIZED FOR RELEASE BY:

Approved on: September 27, 2010
JC-40 Chairman, John Smolka

The following individuals did review/approve the minutes:

Approved on: September 27, 2010
JC-40.1 Sub-Committee Chairman, Rick Williams

Approved on: September 30, 2010
JC-40.3 Sub-Committee Chairman, Ramzi Ammar

Approved on: October 6, 2010
JC-40.4 Sub-Committee Chairman, Jeffrey Chung

Approved on: October 6, 2010
JC-40.5 Meeting Chairman (covering for Mr. Keller), Jeffrey Chung

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Approved on: September 26, 2010
Legal Approval, John Kelly

Approved on: September 26, 2010
Secretary, Mark Kellogg